Exp: Study the functions of a 64 bit RAM.

Theory:

Computer Memory are basically categorized into two (a) Primary memory and (b) Secondary memory.

Primary memory can again be categorized into volatile and non-volatile memory.

Volatile memory loose the content when the power is switched off or removed but the non-volatile memory retains the data stored in memory even after the power is removed.

We will study a RAM size of 64 bit.

The block diagram of a memory module is shown in the figure (1.1)

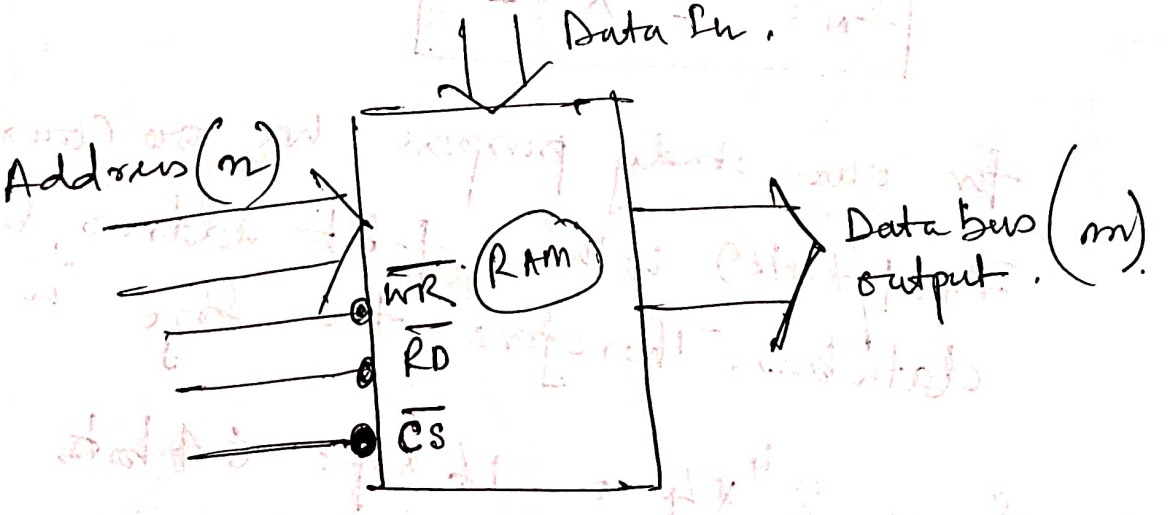

Figure (1.1), Block diagram of a memory.

Let us consider a RAM with a data bus of m bits and Address data bus (n) and control signals, chip select ($\overline{CS}$), read ($\overline{RD}$) and write ($\overline{WR}$). All the control inputs are active low type, i.e when the control inputs are connected to the ground these control signals gets activated.

To calculate the size of the memory we need to know the size of address bus and data bus.

Let S_m be the size of the memory,
Let n be the number of address bits,
Let m be the number of data bits.

∴ Size of memory is;

$$S_M = 2^n \times m$$

For our study purpose we are considering 7489/74189 with 4-bit address bus and data bus. Therefore the size is

$$S_M = 2^4 \times 4 = 16 \times 4 = 64 \text{ bits.}$$

Test Circuit of TTL memory module is shown in the figure (1.2).

The memory IC is a open collector outputs which provide Wire-AND capability.

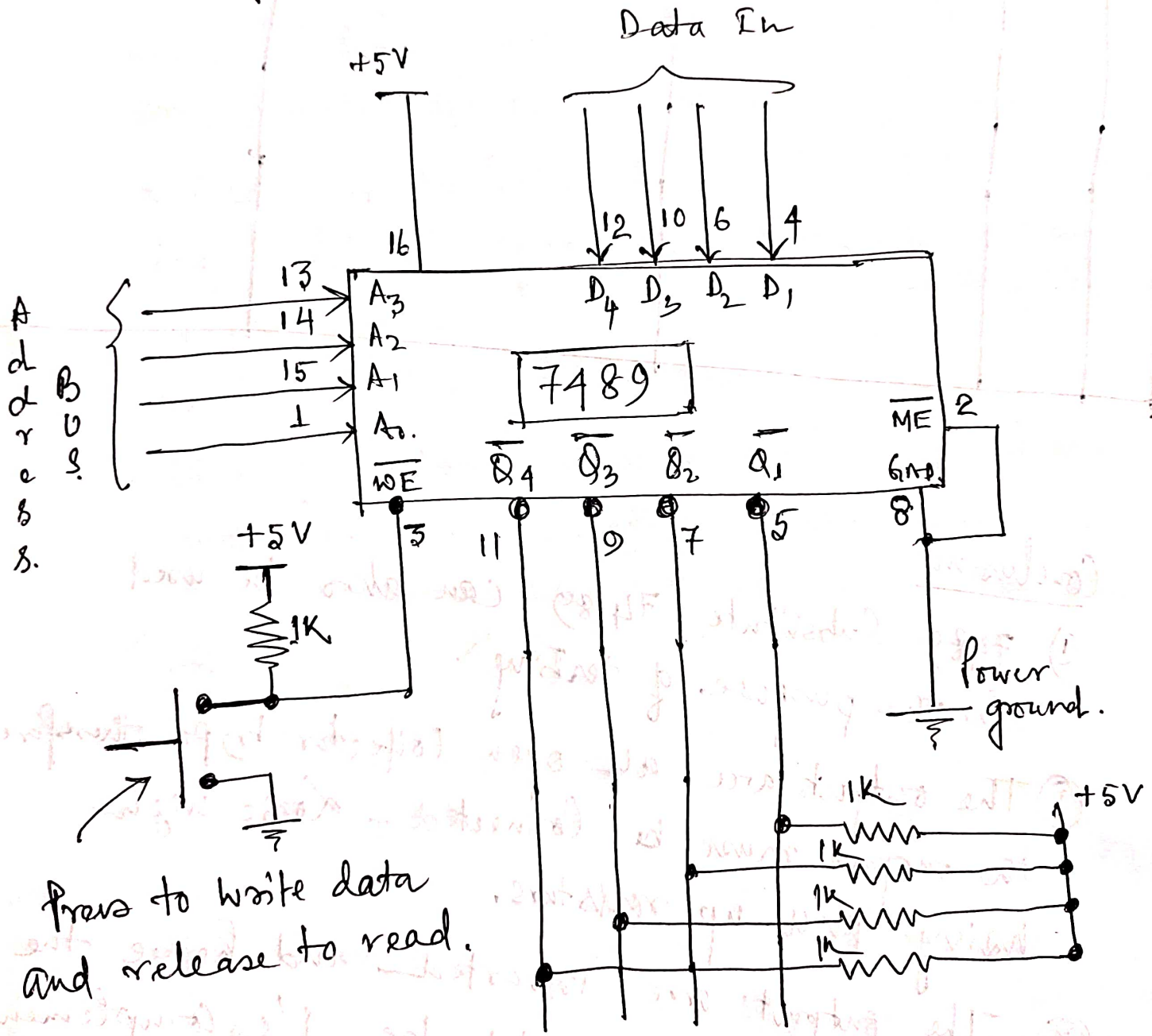

Figure (1.2), Test Circuit for 7489.

Experimental Observation

$\overline{ME}$	$\overline{WE}$	Address Input A_4 A_3 A_2 A_1	Inputs D_4 D_3 D_2 D_1	outputs $\bar{Q}_4$ $\bar{Q}_3$ $\bar{Q}_2$ $\bar{Q}_1$

Conclusion

(1) 7489 Substitute 74189 can also be used for the purpose of testing.

(2) The outputs are all open collector type therefore the outputs must be Connected Logic high having pull-up resistors.

(3) The outputs are inverted and hence the data retrieved would be 1's complement of the actual data inside the RAM chip.

Exp: Horizontal and Vertical cascading of 64 bit RAM and study its output.

Theory: Let us consider a 64 bit RAM which is having 4 bit address and data bus. Since it has 4 bit address bus, there are a total of 16 locations each having a capacity to hold 4 bit of data. Its address space as well as word length can be increased using vertical and horizontal technique.

When the address lines are remain the same and the word length increase we call it Horizontal cascading as shown in the figure (1.1).

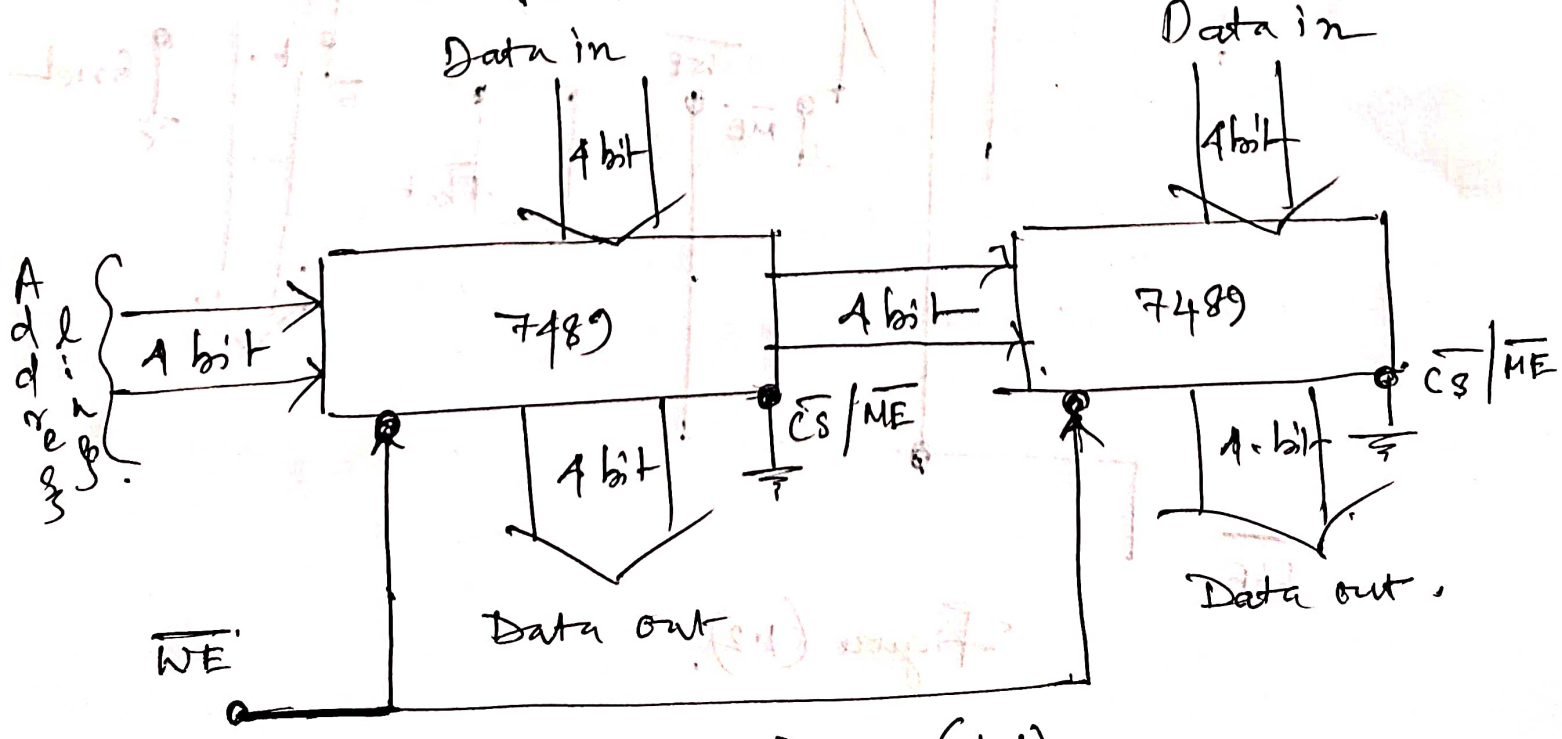

Figure (1.1)

Similarly, when Address space increases including increase in address lines and other remain the same is called vertical Cascading. The block diagram representation is shown in the figure (1.2).

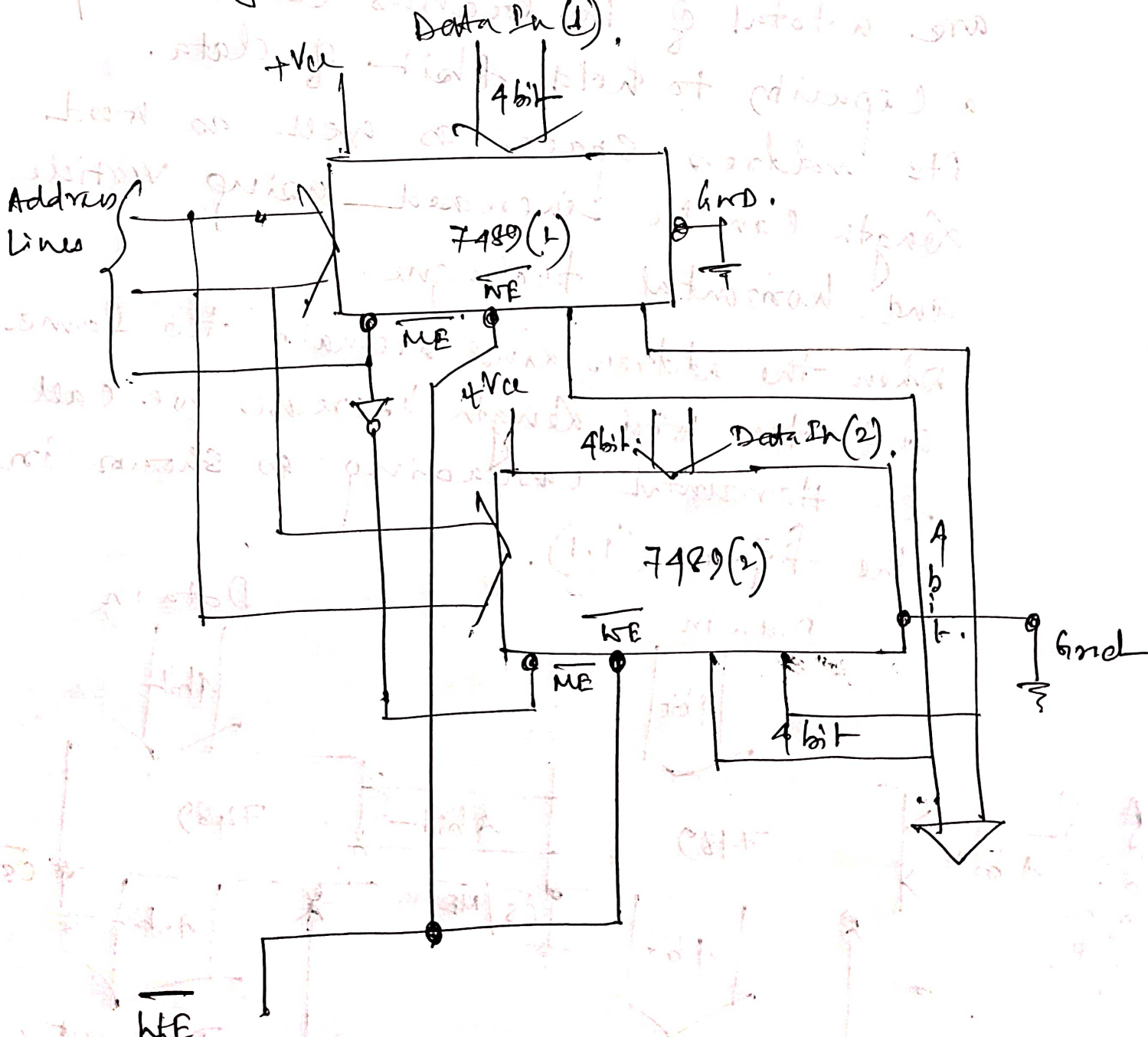

Figure (1.2).

In Vertical Cascading the data inputs of RAM (1) and RAM (2) are tied together along with the data outputs. The Master Enable ($\overline{ME}$) is connected to the ($\overline{ME}$) of the second RAM using a NOT gate to get the MSB of the address line. Now there are 5 address line $\therefore 2^5 = 32$ locations can be addressed. When A_5 i.e the most significant bit is connected to the Logic Low, the RAM 1 gets activated and rest of the bits A_4 to A_1 are used for addressing all the locations of RAM 1. When is connected to Logic high RAM 1 is de-activated and RAM 2 is activated and again A_4 to A_1 is used to address the locations of RAM 2.

Implementation of Horizontal Cascading

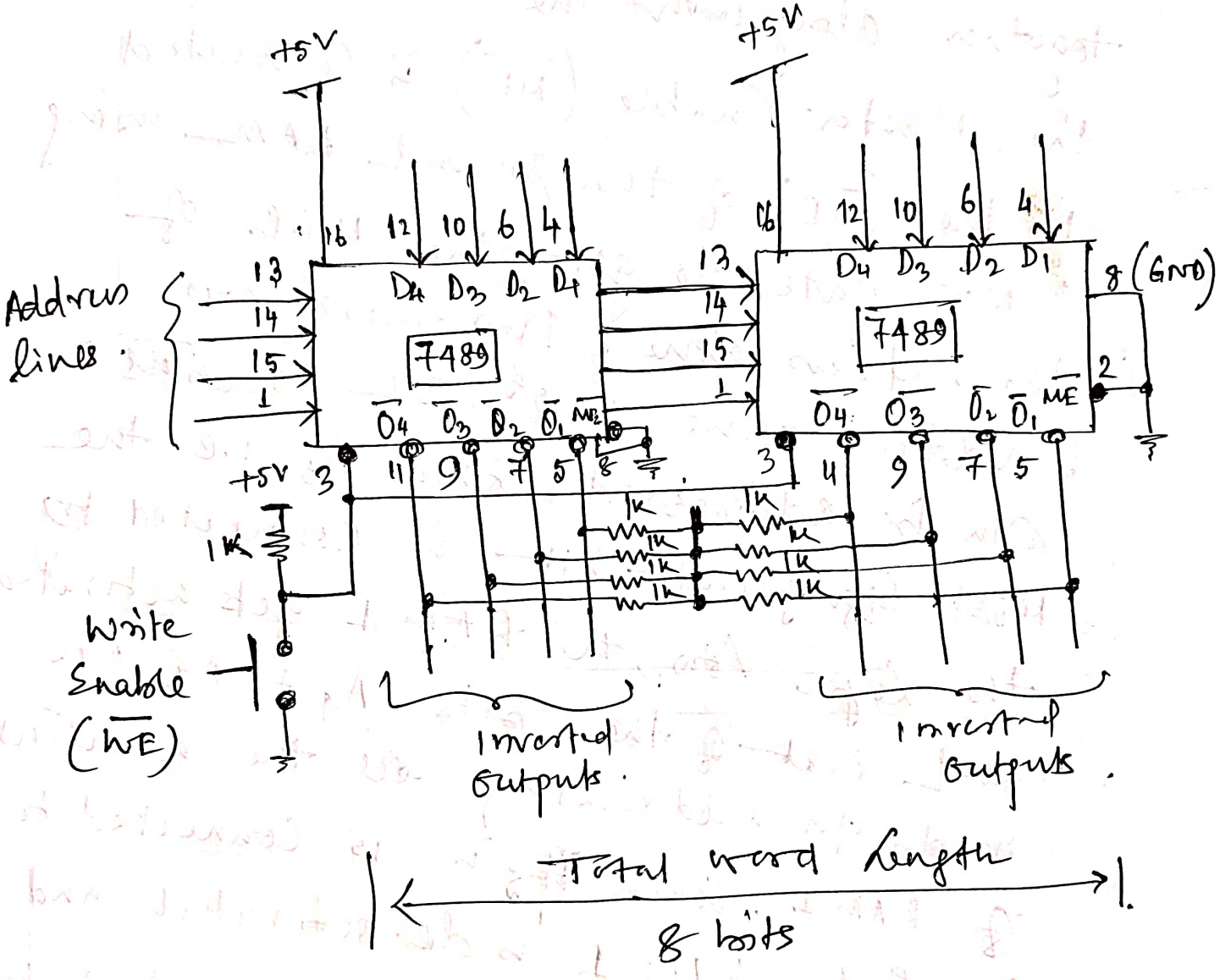

Figure (1.3) Horizontal Cascading.

The vertical cascading of 7489 is shown in the figure (1.4).

Implementation of Vertical Cascading.

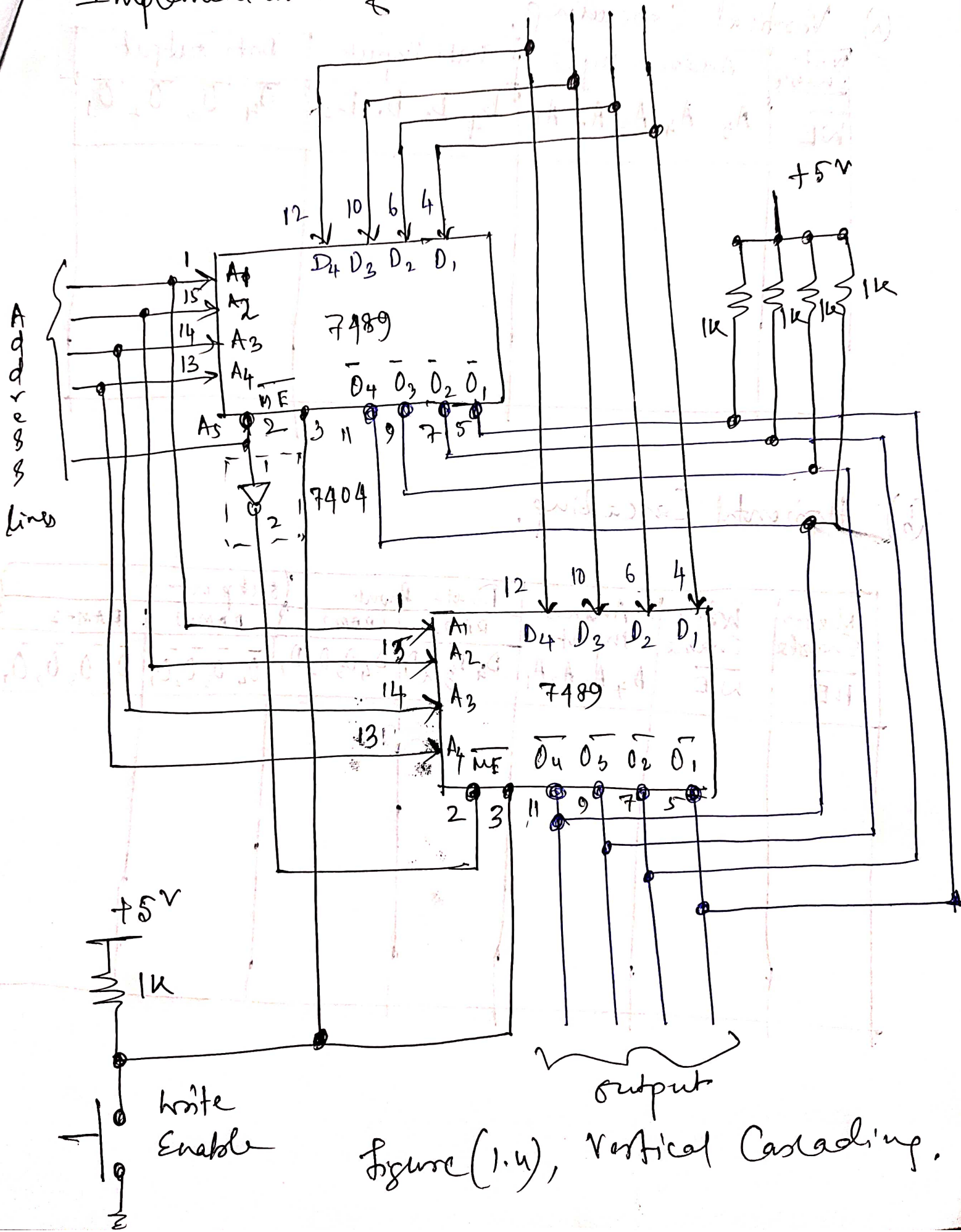

Figure (1.4), Vertical Cascading.

Experimental Observation.

(a) Vertical Cascading.

Write Enable	Address Input	Data Input	Data output
$\overline{WE}$	$A_5\ A_4\ A_3\ A_2\ A_1$	$D_3\ D_2\ D_1\ D_0$	$\overline{O}_4\ \overline{O}_3\ \overline{O}_2\ \overline{O}_1$

(b) Horizontal Cascading.

Master Enable	Write Enable	Address input	Data Input		output	
			RAM 1	RAM 2	RAM-1	RAM-2
$\overline{ME}$	$\overline{WE}$	$A_4\ A_3\ A_2\ A_1$	$D_4\ D_3\ D_2\ D_1$	$D_4\ D_3\ D_2\ D_1$	$\overline{O}_4\ \overline{O}_3\ \overline{O}_2\ \overline{O}_1$	$\overline{O}_4\ \overline{O}_3\ \overline{O}_2\ \overline{O}_1$